Multicore Energy Efficient Scheduling with Energy Harvesting for Wireless Multimedia Sensor Networks

Muhammad Ali Jamshed[1] and *Osama Amjad*[2]

alijamshed107@yahoo.com, osama.amjad@ozu.edu.tr
[1]*Department of Electrical Engineering, Institute of Space Technology, Islamabad, Pakistan.*
[2]*Department of Electrical and Electronics Engineering, Özyeğin University, Istanbul, Turkey 34794.*

***Abstract*—Wireless Multimedia Sensor Networks (WMSNs) are becoming one of the latest trends in the Internet of things. However, in WMSNs the energy constraint is a significant issue. In this paper, an idea of integrating energy harvesting technique with energy efficient scheduling mechanism is proposed. In order to increase the overall energy efficiency, the previously studied scheduling algorithm is used and integrated with a multi-core processor technique. Since increasing the number of cores in a processor decreases the overall energy efficiency, integration of energy harvesting with the processor can alleviate energy loss. The proposed idea constitutes of implementing the technique of lightweight processor (LWP) on a first core and leaving the second core in idle state with multiple lightweight processor implementation. The second core is divided into two parts namely, the main part and the multiple LWPs. The main part of the second core is used to relieve the processing speed issue and the multiple LWPs are used to cover up the flaws of missing deadlines if the number of tasks are increased. The second core comes in operation when the battery capacity is above 50%, using the RF energy harvesting scheme. This method increases the overall energy efficiency of each sensor node from 38% to 60% compared to the single core and single LWP method.**

Keywords*—*wireless multimedia sensor networks, multi-core lightweight processor, energy harvesting, energy efficiency.

I. Introduction

With the advancement in technology such as low power analog and digital devices, embedded microprocessors and wireless communication, has allowed the development of small size and low-cost Sensor Nodes (SNs) which are the basic components of Wireless Sensor Networks (WSNs) [1]. A typical WSN consists of a collection of small autonomous SNs, which collect the data such as temperature/humidity, light, pressure etc. from surrounding environment or certain geographical areas and pass the sensed data to the main location or master node. Every device in a WSN consists of a radio transceiver with an internal or external antenna for wireless communication, an energy source which is usually a battery or a connecting energy harvesting device and usually a data processing unit known as the microcontroller. Currently, WSNs have a wide range of interesting applications in different areas including civil and military applications, energy saving smart grids, medicine and healthcare, disaster relief operations, biodiversity mapping, industrial and household monitoring [2].

Recently with the development of low-cost multimedia hardware such as complementary metal-oxide semiconductor (CMOS), video camera and miniature microphones, the research trend is shifting towards the usage of Wireless Multimedia Sensor Networks (WMSNs). It can be defined as the network of wirelessly connected SNs equipped with multimedia hardware, such as cameras that enables the capturing of audio and video streaming, scalar sensor data and still images [3]. Fig. 1 shows the general architecture of WMSNs. The CMOS chip is inserted into a specific device, for example, a lens, the logic components and optic sensors that are used in processing the digital signals by executing the algorithms, such as the ones that are used for compression and stabilization of images [4]. As an example, the interference and image-capturing cyclops modules [5], designed for highly lightweight imaging, can be connected with wireless sensors such as MICA2 or MICAz, Crossbows, thus realizing a multimedia connection with imaging acquisition and with processing and transmission functionalities. With the emergence of WMSNs, a new perception has been opened to the existing WSNs thereby increasing its capacity (by incorporating inexpensive hardware) and intended applications; e.g. multimedia surveillance sensor networks are used to upgrade and complement current surveillance systems to prevent criminal and terrorist activities, intelligent transportation system (ITS) is used to monitor road traffic in big cities and to deploy services that offer routing strategies to avoid traffic congestion and violations, etc. [6].

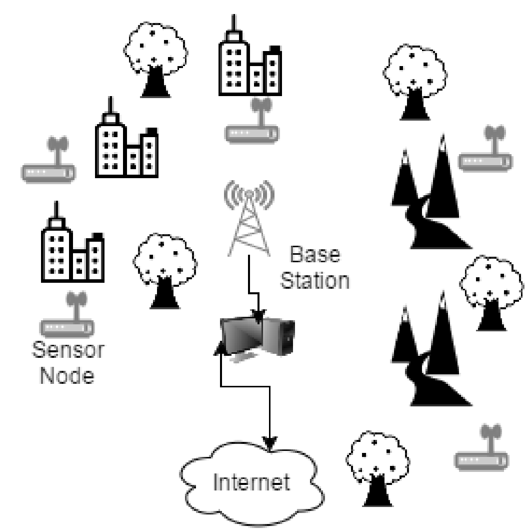

Fig. 1: A general diagram for wireless multimedia sensor networks conveying information to central unit.

With the development of WMSNs, the challenges associated with the typical WSNs have also increased. With the addition of multimedia content, video, audio, and still images, the

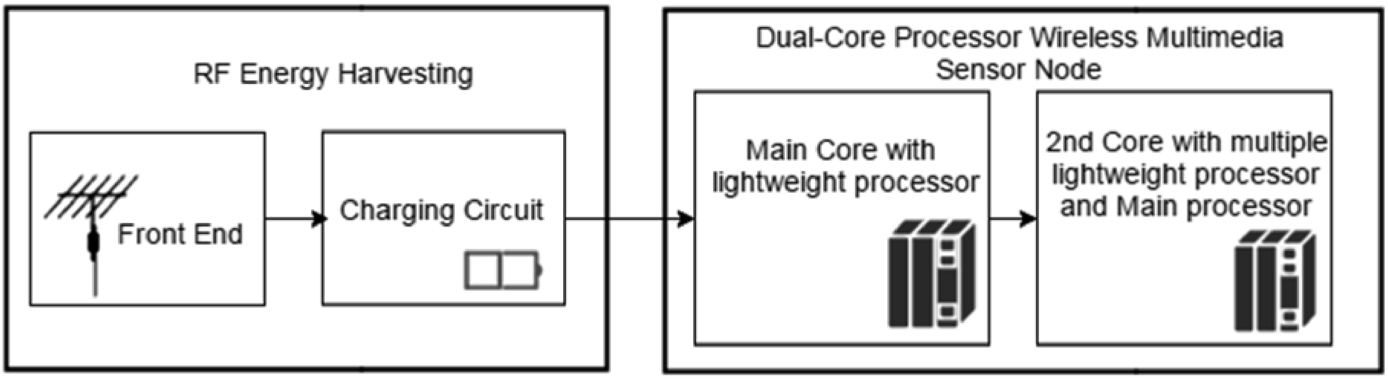

Fig. 2: An overall architecture of proposed integrated scheduling and energy harvesting system.

sensor network architecture need to be reconsidered to provide a satisfactory level of Quality of Service (QoS). Moreover, along with the previous research challenges associated with the WSNs such as scalability, limited computational power, etc. additional research challenges such as application specific QoS guarantee, coverage area, minimized energy consumption, increased bandwidth requirement, etc. are needed to be taken into account. In this regard, significant research efforts have been done to maintain an application specific QoS.

A. Related Work

A QoS-oriented high efficiency resource allocation scheme which introduces a comprehensive search method to obtain an optimal scheduling sequence and corresponding transmission method for deadline constrained multimedia transmissions in WSNs has been proposed in [7]. In [8], a new congestion control method for transmitting the video stream in WSNs has been proposed to improve the QoS. The node-level optimal real-time priority based energy efficient dynamic scheduling algorithm has been proposed in [9], which schedule the tasks according to the priorities by increasing or decreasing the frequency. An energy efficient scheduling mechanism has been proposed in [10], which introduce the concept of Lightweight Processors (LWPs) to limit the size of each node, without compromising on task integrity. RF energy harvesting, on the other hand, is an interesting research area that has been significantly used in academics and industry. It can be used to empower the low-power devices such as IoT, WSNs, etc. In [11], an RF energy harvesting system for Wireless Local Area Network (WLAN) sources operating at 2.4 GHz and 5.8 GHz has been designed and analyzed.

The previous work on WMSNs in [10] only considers the scheduling mechanism by utilizing the concept of the LWP to increase the life period of the WMSN and to maintain a specific QoS. However, the proposed algorithm in [10] caters the flaws of the early algorithm in [9], but induces a less processing speed and becomes unstable by increasing the number of tasks. The present work focuses on the energy efficiency of the system by introducing a dual-core processor and proposing an idea of integrating it with RF energy harvesting system [11]. By using this concept, the overall processing speed of each SN is shown to be increased and their multiple task handling capability is enhanced. The main objectives of the paper can be summarized as follows:

- To propose an integrated scheduling and energy efficient architecture for WMSNs in order to overcome the less processing speed issue of single core processors.
- To enhance the capability of a single WMSN to multitasking in order to overcome the missing of task deadline if the number of tasks is increased.
- To increase the overall lifespan of each SN using energy efficiency as a metric with the integration of energy harvesting concept.

The remaining paper is organized as follows: In Section II, the overall architecture of the proposed system model has been described and discussed in detail. Section III presents the proposed integrated energy scheduling and harvesting algorithm and the pseudo-code that explains the working principle of the algorithm. Section IV presents the simulation results and the analysis of the proposed mechanism. Finally, Section V gives the conclusions.

II. System Model and Architecture

The overall architecture of the proposed mechanism consists of two major systems: RF energy harvester unit and wireless multimedia sensor node with the dual-core processor. The RF energy harvesting utilizes an efficient receiving antenna which captures RF signal from the surrounding environment and converts them into functional DC power. The harvested energy is used to charge the rechargeable battery of a SN present in the storage circuit. The second sub-system of the proposed architecture consists of a multimedia sensor node that utilizes a dual-core processor to schedule the tasks using energy efficient algorithms as proposed in [9] and [10] with an enhancement of energy harvester and multiple LWPs on a second core to resolve the flaws of less processing speed and multiple task handling capability.

Fig. 2 shows the block diagram that describes the overall concept and brief overview of our proposed system model. The front end receiving antenna operating at specific frequency captures the ambient RF signals, which are rectified to DC output power by the voltage rectifier block. The harvested energy is supplied to the rechargeable battery of the SN and the remaining block constitutes processor of WMSN. The processor that has been proposed in this paper consists of two cores. The first core/main core consists of a single LWP and the main processor. The second core consists of multiple LWPs, which depends upon the number of tasks being handled by the processor, and the main processor. The main processor plays its role in the scheduling of the tasks along with the main part of the first core. The second core sits in idle state and comes in operation when the battery capacity is above 50% of the total power storage. These factors motivate us to develop an energy efficient scheduling mechanism, which caters all of them.

III. Integrated Energy Scheduling and RF Energy Harvesting

A WMSN consists of a network of small spatially distributed autonomous SNs that are equipped with inexpensive hardware to monitor the geographic conditions. Each device in a network gathers the multimedia data and scalar sensor data from the surrounding environment or certain geographical area and pass the collected information to the central location or sink node.These nodes operate on batteries and cannot be fed by external power source. We need energy efficient algorithms to maintain the QoS for multimedia applications. These algorithms are deployed at each sensor node that controls the use of energy locally as well as globally.

Flowchart and pseudo code of the proposed algorithm can be seen in Fig. 3 and Algorithm 1 respectively. The flowchart helps to analyze the proposed scheduling algorithm in detail. It draws a clear picture of the list of operations performed in a given sequence. The flowchart in Fig. 3 has been explained in detail with the corresponding numbers on the flow diagram. Referring to the step 1 and 2, the algorithm starts and set the priorities after reviewing the input data. The flow step 3 and 4 performs the processor division. Furthermore, the condition of tasks confronting is managed by shifting the lowest priority task (ϕ) on LWP and performing the highest priority task (σ) on the main processor. The Dynamic Voltage Frequency Scaling (DVFS) helps in ceasing the priorities and scales the processor as per need. This is being performed in step 5, 5a and 5b. A condition on battery capacity has been applied in step 6 to check whether to use a single core (6a) or both the cores (6b), to perform scheduling. A pseudo-code version of the flowchart has been given in Algorithm 1.

In Table I, the symbols we used throughout the Algorithm 1 and paper are presented. In the proposed algorithm named as Multicore Scheduling with RF Energy Harvesting (MSEH) in Algorithm 1, starting from line 1, MSEH takes ϵ (Number of tasks), $\mathbf{\Gamma}$ (Deadline) and $\mathbf{\Theta}$ (Execution time) as input parameters, for defining tasks priorities. The line 3 - 8 initiates a loop for the duration of ϵ (number of tasks). This loop checks for least and most values from $\mathbf{\Gamma}$, and based on that, the algorithm sets the priorities in terms of σ (highest priority) and ϕ (lowest priority). In line 9 and 10, the evaluation of Ω_1 (processor core) is performed. The Ω_1 is set as main core and is further divided into two parts, the main processor, containing major portion and a LWP. The division is performed in a ratio of 9:1. The LWP makes sure that the integrity of each ϕ is maintained. Line 11 starts the evaluation of Ω_2. Further line 12 makes Ω_2 as a standby core. The line 13 divides Ω_2 into (ϵ-2) multiple LWPs and a half in the main processor. The multiple LWPs will help to maintain the integrity of each ϕ if ϵ increases. The main processor will play its part to cover up the less processing speed issue. Further moving to line 14, a loop is initiated for a duration of α (battery storage) which performs scheduling till α expiration. Referring to line

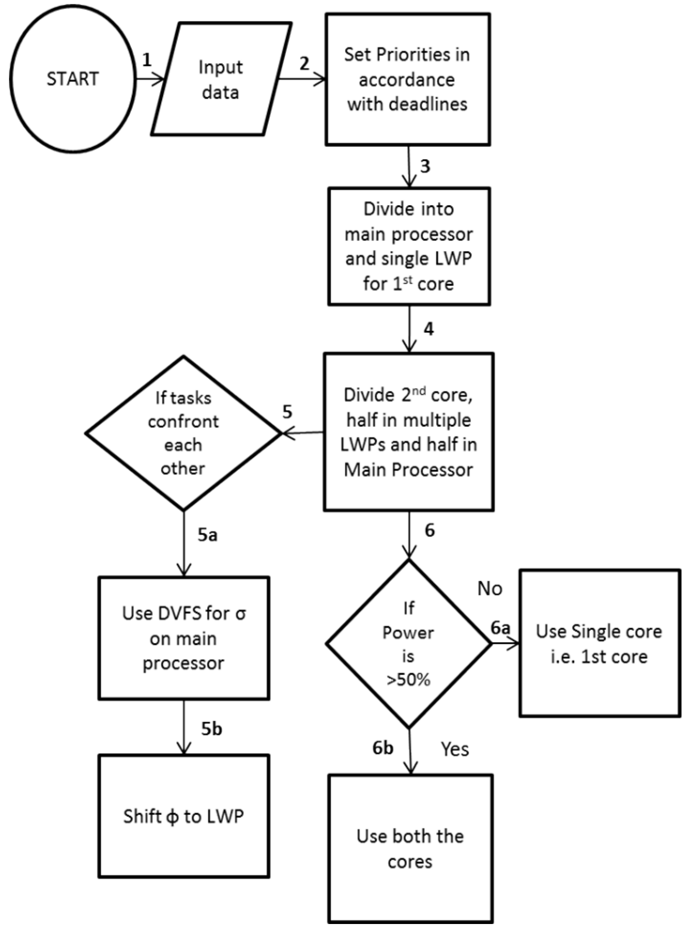

Fig. 3: Flow chart of proposed scheduling mechanism for WMSN.

15, the execution of the tasks begins, based on $\mathbf{\Theta}$. Line 16 decrements α after each task processing based on ζ, δ, γ and β. In line 17 and 18, there is check for battery capacity, which increases the lifespan of each SN. According to the algorithm, if the battery capacity is above 50%, full utilization of dual-core processor is possible otherwise only single processor will be in operation. Furthermore, in line 20, if the condition of $\sigma = \phi$ is met, the method of DVFS comes into effect and it does not allow these static priorities to be changed during run-time as compared to earliest deadline first (which is a dynamic scheduling algorithm, that changes the priorities of tasks on run-time). The ϕ is shifted to LWP and σ is performed on the main processor. In line 22 the loop gets terminated upon battery expiration and referring to line 23, the algorithm procedure gets terminated. Finally, with the MSEH algorithm, we come to the conclusion that the full utilization of dual-core processor is possible only when the power capacity of the battery, attached to the SN is above 50%.

IV. Simulation Results

In this section, a detailed parametric analysis has been performed using MATLAB software. We have assumed that each processor attached to SN has a frequency of 20 Hz each. The $\zeta = 0.1$ J is assumed to schedule each task. All the observations related to the task scheduling are done till first η. The algorithm has been run for N = 6 tasks with the above assumptions that each task having a particular value from $\mathbf{\Theta}$. The $\mathbf{\Theta}$ for each task is [2, 1, 2, 2, 3, 4] sec, whereas $\mathbf{\Gamma}$ is

Algorithm 1 Multi-core Scheduling with RF Energy Harvesting (MSEH)

procedure INPUT(ϵ, $\mathbf{\Gamma}$, $\mathbf{\Theta}$)
  Set tmp = $\mathbf{\Gamma}[1]$, $i = 1$;
  for $i \leq \epsilon$ **do**
    if ($\mathbf{\Gamma}[i] < tmp$) **then**
      Set $\sigma = \mathbf{\Gamma}[i]$ and $tmp = \sigma$
    else
      Set $\phi = \mathbf{\Gamma}[i]$ and $tmp = \phi$
    end if
    Increment i
  end for
  Evaluate Ω_1 using LWP.
  Set Ω_1 to main core.
  Evaluate Ω_2.
  Set Ω_2 to standby core.
  Divide Ω_2 with half main core and half in (ϵ-2) LWPs.
  while ($\alpha > 0$) **do**
    Execute tasks based on $\mathbf{\Theta}$
    Decrement α based on ζ, δ, γ and β
    if (α >50%) **then**
      utilize Ω_1 + Ω_2
    else
      utilize Ω_1
    end if
    if σ == ϕ **then**
      Execute σ by DVFS.
      Shift ϕ to LWP.
    end if
  end while
end procedure

TABLE I: Symbols used throughout the paper

Symbol	Meaning
$\mathbf{\Gamma}$	$1 \times \epsilon$ deadline vector of all tasks
$\mathbf{\Theta}$	$1 \times \epsilon$ execution time vector of all tasks
ϵ	Number of Tasks
σ	highest priority task
ϕ	lowest priority task
$\mathbf{\Omega}$ = (Ω_1, Ω_2)	Processor with two cores
α	Battery storage
η	hyper period
ζ	energy consumption for 1 sec
δ	DVFS energy consumption
γ	Single LWP activation energy
β	Initial energy consumption

selected to be [3, 4, 5, 6, 7, 8] sec. Battery requirement is 84 J to observe the trend of N = 6 tasks over a complete η which is in accordance with the $\zeta = 0.1$. The $\eta = 840$ sec for the N = 6 tasks with their corresponding values from ($\mathbf{\Gamma}$). An additional energy of $\delta = 0.2$ J is required for DVFS. Furthermore, for performing single LWP activation, $\gamma = 5$ mJ of more energy is required. An additional $\beta = 0.5$ J is further required to set task priorities and processor division. The energy efficiency is calculated in % using the ratio of output energy consumed and input energy provided by the battery. The input energy is same as mentioned above whereas the energy consumed to schedule these periodic tasks over the first η is the output energy. The battery capacity is set according to assumed energy consumption per second and calculated per η.

According to the above mentioned assumptions, the simulations have been performed, first using the algorithm in [10] which uses single core and a single LWP. Fig. 4 shows the trend of energy efficiency versus processing speed for the different number of tasks. It can be noticed that the output energy efficiency is observed to be 38% for N = 6 number of tasks and at a fixed processing speed of 6 Hz. Moreover, it can be noticed that the energy efficiency shows a decreasing trend with the processing speed. This is due to the fact that as we move further in time the chance of tasks confronting each other increases. Therefore, the processor increases the processing speed as it needs to use the DVFS and LWP switching at an increased rate. Subsequently, this decreases the overall energy efficiency. Moreover, the processor is unable to schedule these tasks for a complete η with the provided battery ratings. Therefore the task handling capacity of the CPU decays at a much faster rate by increasing the processing speed and number of tasks.

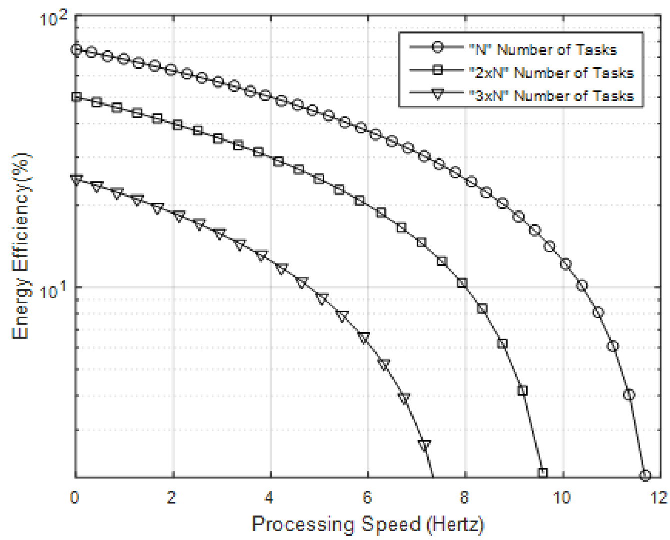

Fig. 4: Energy efficiency vs. processing speed for different number of tasks.

To overcome the issue, the simulations have been repeated again with the proposed MSEH algorithm that includes an energy harvesting mechanism along with the addition of a dual-core processor. Using this mechanism, the overall task handling capacity of each sensor node is increased. The dual-core mechanism and multiple LWP require more energy but the addition of energy harvester mitigate this problem. It can be seen in Fig. 5 that for a constant processing speed of 6 Hz, the output energy efficiency of the system is increased to 60%, 40%, and 25%, for N, 2N and 3N number of tasks in comparison to a single core and a single LWP respectively. Moreover, it is noticed that by integrating the energy harvesting mechanism, the overall trend of energy efficiency remains same as that of Fig. 4.

Fig. 6 shows the comparison of the proposed MSEH with the algorithm that uses a single LWP with a single core. It can be seen that the task handling capacity of each SN with single core processor decreases by increasing the number of tasks. The node can process at a maximum of 14 tasks only, after that the efficiency of the single core completely decays. On the

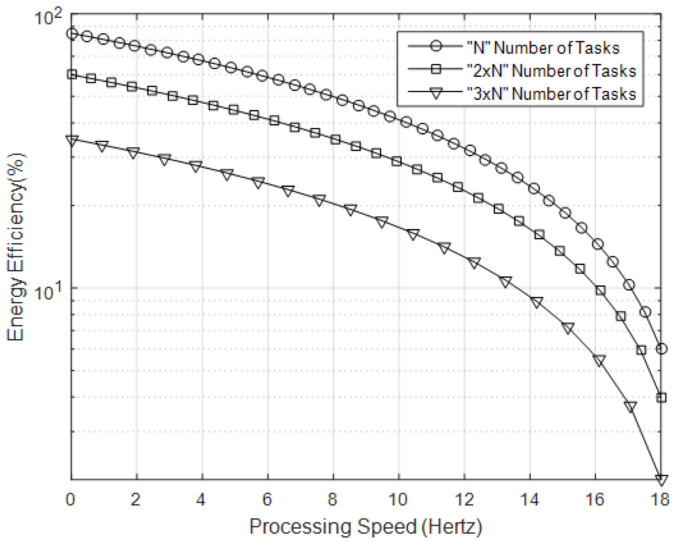

Fig. 5: Energy efficiency vs. processing speed with the addition of energy harvesting charging circuit.

other hand, by using the proposed MSEH algorithm, the task handling capacity of the SN is significantly increased. It can be noticed that by using a MSEH method, the node can handle even 25 tasks with an energy efficiency of approximately 15%.

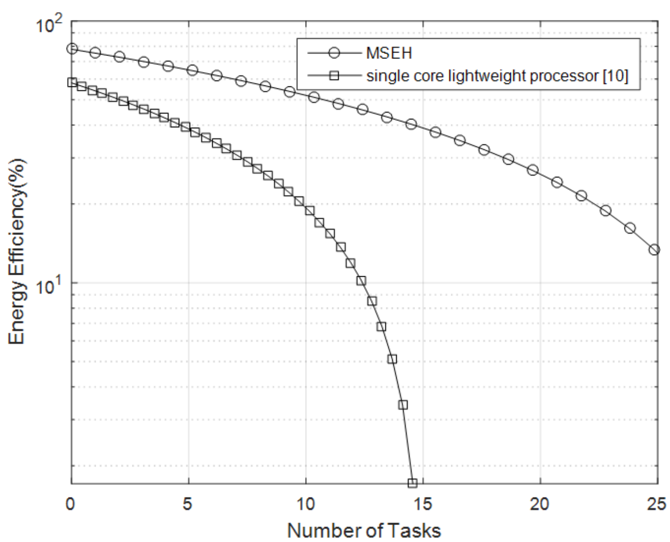

Fig. 6: Efficiency of multi-core scheduling with energy harvesting (MSEH) in comparison with single LWP.

V. Conclusion

In this paper, an energy efficient scheduling mechanism with the integration of energy harvester and dual-core processor technique has been proposed. The use of a dual-core processor has equipped each SN with a platform to cover up the issue of less processing speed. If the number of task increases, the multiple LWPs caters the missing of deadlines of lowest priority tasks. There is a considerable increase of 22% efficient use of energy in comparison to a single core with single LWP. By increasing the number of processors for a single SN, the overall cost and size of each SN increases. The existence of 50% check on battery capacity is necessary because energy harvester is unable to cover the intense data applications of WMSNs. Using this check on battery, limits the algorithm performance, but relatively increases the lifespan of each SN. Hence our proposed mechanism is energy efficient, but it should also be noted that there can be performance drawbacks due to virtualization.

References

[1] S. Ehsan and B. Hamdaoui, "A survey on energy-efficient routing techniques with qos assurances for wireless multimedia sensor networks," *IEEE Communications Surveys & Tutorials*, vol. 14, no. 2, pp. 265–278, 2012.

[2] Y. A. U. Rehman, M. Tariq, and T. Sato, "A novel energy efficient object detection and image transmission approach for wireless multimedia sensor networks," *IEEE Sensors Journal*, vol. 16, no. 15, pp. 5942–5949, 2016.

[3] I. F. Akyildiz, T. Melodia, and K. R. Chowdury, "Wireless multimedia sensor networks: A survey," *IEEE Wireless Communications*, vol. 14, no. 6, 2007.

[4] L. A. Grieco, G. Boggia, S. Sicari, and P. Colombo, "Secure wireless multimedia sensor networks: a survey," in *Mobile Ubiquitous Computing, Systems, Services and Technologies, 2009. UBICOMM'09. Third International Conference on*, pp. 194–201, IEEE, 2009.

[5] M. Rahimi, R. Baer, O. I. Iroezi, J. C. Garcia, J. Warrior, D. Estrin, and M. Srivastava, "Cyclops: in situ image sensing and interpretation in wireless sensor networks," in *Proceedings of the 3rd international conference on Embedded networked sensor systems*, pp. 192–204, ACM, 2005.

[6] A. Sharif, V. Potdar, and E. Chang, "Wireless multimedia sensor network technology: A survey," in *Industrial informatics, 2009. INDIN 2009. 7th IEEE international conference on*, pp. 606–613, IEEE, 2009.

[7] L. Guo, Z. Ning, Q. Song, L. Zhang, and A. Jamalipour, "A qos-oriented high-efficiency resource allocation scheme in wireless multimedia sensor networks," *IEEE Sensors Journal*, 2016.

[8] N. Borzouie and N. Borzouie, "Improve the quality of services to help congestion control flows to send a video in wireless multimedia sensor networks," in *Information and Knowledge Technology (IKT), 2016 Eighth International Conference on*, pp. 241–246, IEEE, 2016.

[9] M. A. Jamshed, M. F. Khan, K. Rafique, M. I. Khan, K. Faheem, S. M. Shah, and A. Rahim, "An energy efficient priority based wireless multimedia sensor node dynamic scheduler," in *High-Capacity Optical Networks and Enabling/Emerging Technologies (HONET), 2015 12th International Conference on*, pp. 1–4, IEEE, 2015.

[10] M. A. Jamshed, A. Nauman, M. F. Khan, and M. I. Khan, "An energy efficient scheduling mechanism using concept of light weight processors for wireless multimedia sensor networks," in *Applied Sciences and Technology (IBCAST), 2017 14th International Bhurban Conference on*, pp. 792–794, IEEE, 2017.

[11] S. W. Munir, O. Amjad, E. Zeydan, and A. Ö. Ercan, "Optimization and analysis of wlan rf energy harvesting system architecture," in *Wireless Communication Systems (ISWCS), 2016 International Symposium on*, pp. 429–433, IEEE, 2016.